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MEMS THERMOELECTRIC MICROCOOLER

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Abstract

We report prototype thermoelectric microcoolers (μ-TEC) based on transport along thin- and thick-film plane using MEMS technology. Described is the fabrication processes as well as an analytic model used to design the microdevices. Si/Ge superlattice thin films grown by MBE and electrochemically deposited Bi_2Te_3 films are used as the thermoelectric materials in the fabrication of the μ-TEC. To reduce the heat leakage, the substrates are removed under the active region such that the cooling spots are suspended only by the thermoelectric legs. Additional heat leakage through the supporting structure and thermal radiation are considered through modeling.

I. Introduction

Progresses have been made in the last few years in the development of new materials, particularly superlattice structures, with enhanced figure of merit (ZT) [1]. Thermoelectric microcoolers (μ-TEC) made of such thin films are potential candidates for the thermal management and temperature stabilization of certain electronic and optoelectronic devices [2]. Approaches to fabricate devices based on thin-film materials are being explored. In general, there are two types of device configurations. In the first type, the current and heat flow perpendicular to the film plane, i.e., the cross-plane device. This configuration is similar to devices made of bulk materials. In the second type of devices, i.e., the in-plane devices, the heat and current flow parallel to the film plane. For the in-plane devices, an increase in Z has been calculated to arise from a number of factors, including an increase in the electronic density of states for small well widths (several nanometers), as well as an increase in the carrier mobility if modulation doping is exploited [3]. A potential difficulty to obtain high performance devices is that the inert spacer or supporting material does not contribute to the Peltier heat flow, but does allow heat leakage that lowers the effective ZT of the structure. In the cross-plane device, thermionic emission and phonon thermal conductivity reduction have been conjectured as the possible ZT enhancement mechanisms [4-6]. Significant thermal conductivity reductions in both in-plane and cross-plane directions in quantum structures have been theoretically predicted and experimentally observed [7]. In the device area, thin film devices based on transport in both directions are being pursued, with each having its own advantages and disadvantages. The cross-plane devices face the challenge of establishing a large temperature difference across thin films of a few μm thick. The in-plane devices face the issue of heat leakage through the supporting substrate, which this paper addresses.

Our approach in developing the μ-TEC is to design the microfabrication in such a way that MEMS processes are not significantly affected by how the TE films are prepared, so that more advanced TE materials can be adopted readily in the future. The schematic view of μ-TEC, illustrated in Fig. 1, is used for analysis and device fabrication. The TE elements are not only the thermoelectric components, but are also the supporting components for the cooling spot membrane. By applying current into the system, the cold spot membrane becomes cooler, and the frame functions as a heat sink. From the analytic model [8], the performance of devices is predicted and used to identify the major problems associated with the devices and their solutions. Fabrication process of μ-TEC is developed based on the simulation results.

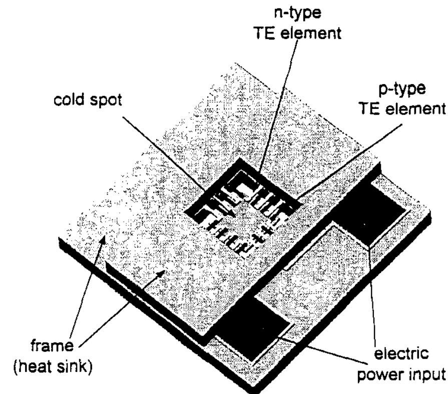

Figure 1. Concept of thermoelectric microcooler (μ-TEC).

II. Analytic model of μ-TEC

The microdevice includes 4n pairs (n-type and p-type) of TE legs (width b and length l) connected in series, as shown in Fig. 1, bridging the cold spot membrane (temperature T_c) around cooling region (area F) to the frame rim (temperature T_∞). The thickness of the TE leg is limited by the thin-film deposition technologies, which is currently on the order of μm's or less. Therefore, the temperature distribution in the thickness direction can be ignored. Furthermore, because of the symmetric design of the μ-TEC, analysis of one pair of the TE legs, shown in Fig. 2, is sufficient to predict the performance of the entire device [8]. The analytic solution is given by:

$$(T_c - T_\infty)[\frac{k_f t_f b}{l}\frac{s}{f(s)} + \gamma_F \frac{F}{4n}] = -[(\alpha_n - \alpha_p)IT_c - N] + I^2\{R[\frac{g(s)}{sf(s)}] + R_{ec}\} \quad (1)$$

where k_f and α_i denote the thermal conductivity and Seebeck coefficient of thin TE films, respectively, and subscripts n and p represent n-type and p-type, respectively. R_{ec} is the specific electrical contact resistance (ranging from 10^{-6} to 10^{-8} Ωcm^2). The heat transfer coefficient is defined as $\gamma_F = 2\beta + 8\varepsilon\sigma T_\infty^3$, where β is the natural convection coefficient of the surrounding air, ε is the emissivity of the TE legs, and σ is the Stefan-Boltzmann constant. Shape parameters are defined by $s = l\sqrt{p}$ with $p = \gamma / k_f t_f$, and functions $f(s)$ and $g(s)$ are defined as

$$f(s) = \tanh(s) \quad (2)$$

$$g(s) = 1 - \frac{1}{\cosh(s)} \quad (3)$$

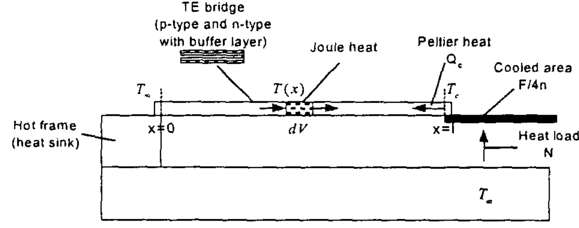

Figure 2: Analytic model of μ-TEC.

To accommodate various types of TE films, the TE film deposition is placed at the beginning of whole process flow. The rest of fabrication processes are designed in such a way that do not damage or degrade the TE films. With patterning technique depending on the film type and deposition method and n- and p-type TE legs having the same shape, the thickness will be the major factor for the performance of μ-TEC. Two types of materials, thin-film Si/Ge superlattice grown by MBE and thick film Bi_2TE_3 grown by electroplating technique [9], are used for making μ-TEC. The following sections will predict the performance and develop the fabrication processes for these two kinds of μ-TEC separately.

III. Thin film Si/Ge superlattice μ-TEC

The Si/Ge superlattice film we used have 100 periods of 20 Å Si/20 Å Ge, designed based on theoretical modeling and some existing experimental data [10,11]. TE legs are made from the n-type and p-type Si/Ge superlattice films with a buffer layer (thickness t_b) deposited by molecule beam epitaxy (MBE). This layer has continuously graded silicon concentration from 100% Si at the substrate interface to $Si_{0.5}Ge_{0.5}$ at the region where the superlattice growth commences [11,12]. Because this MBE-deposited TE film is only around 0.4 μm, the resistance of the TE legs is large enough to neglect the electric contact resistance, shown in Eq. (1).

The exact figure-of-merit values of the superlattices are unknown. We assumed ZT=1 to identify potential problems. Using other relevant properties, the performance of μ-TEC is plotted in Fig. 3 (operating in vacuum) and Fig. 4 (operating in air environment). With the same size of cooling region (1 mm^2), the temperature difference or cooling capacity can be found to be dependent on the occupancy of TE pairs around the cooling region, which can be defined by the occupancy ratio (C) multiplied by perimeter of cooling region. The buffer layer degrades the performance of Si/Ge μ-TEC significantly and thus should be removed. The heat transfer coefficient γ_F, used to gauge the performance degrading by the heat leakage through air, indicates better performance operating the μ-TEC in vacuum.

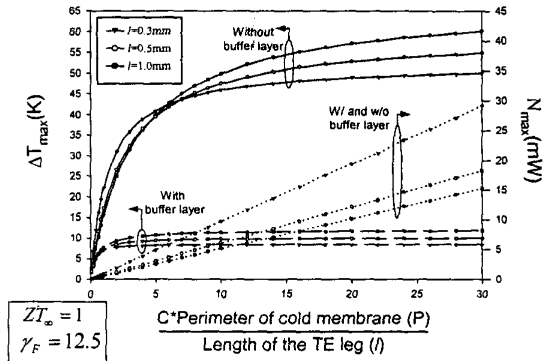

*Figure 3: Performance of the μ-TEC as function of C*P/l operating in vacuum*

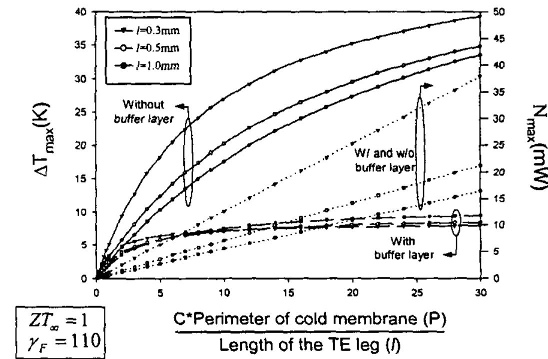

*Figure 4: Performance of the μ-TEC as function of C*P/l operating in air environment*

Based on the simulation result, the fabrication of μ-TEC is designed. After Si/Ge superlattice film is grown by MBE, the film patterning is achieved by fluorine-based reactive ion etching (RIE). According to the measurement on patterned sample by atomic force microscope shown in Fig. 5, the selectivity ratio between Si/Ge and Si or SiO_2 is found to be around 6:1.

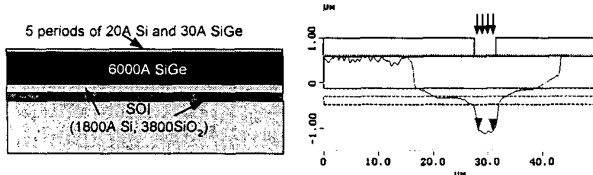

Figure 5: Test of Si/Ge patterning (a) Sample preparation (b) AFM measurement after F-RIE patterning

The film patterning by F-RIE is tested on both n-type and p-type Si/Ge superlattice films, as shown in Fig. 6. The designed width of TE legs is 20 μm, 50 μm, and 100 μm. The function of C*P/l, on the performance in Figs. 3 and 4, can be calculated to be 0.3, 0.8, 1.7, respectively. To ease fabrication, the current design of TE leg patterns does not aim for the device performance optimization, which can be improved by minimizing the space between TE pairs or maximizing the number of TE pairs in the future. The fabrication process, designed by MEMS technology, will be described in Section V.

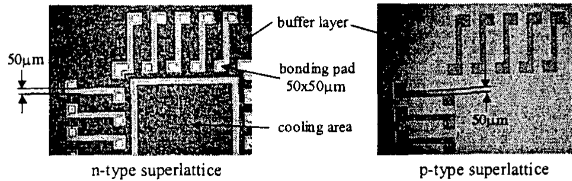

Figure 6: Si/Ge leg patterns made by F-RIE.

IV. Thick film Bi_2Te_3 μ-TEC

Another high ZT material, Bi_2Te_3, grown by electroplating technique at JPL, is used for μ-TEC fabrication. The thickness of plating TE material is limited by the mold, which can be made by thick photoresist ranging from μm's to over 100 μm. By using the analytic model built in Section II, the performance of μ-TEC can be predicted in Figs. 7 and 8 in terms of thickness of TE pairs.

Without considering the electric contact resistance effect, both temperature (Fig. 7) and cooling capacity (Fig. 8) enhance with the increasing film thickness, as also shown by Volklein [13]. However, unlike Si/Ge superlattice μ-TEC, the electric contact resistance becomes relatively important as the resistance of TE pairs decreases with increasing thickness of the electroplated TE film. To ensure good performance of μ-TEC, the desired thickness of both n- and p-Bi_2Te_3 film are 5-10 μm. In Fig. 9, leg patterns of 10 μm-thick electroplated n-Bi_2Te_3 film is ready for the μ-TEC fabrication. Most of the device fabrication processes can be used for either thin or thick TE films, which will be described in the following section.

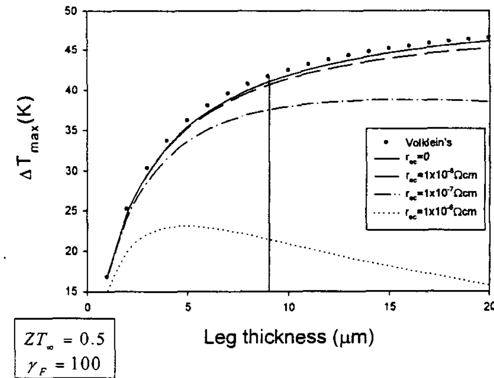

Figure 7: Temperature difference of the μ-TEC as function of thickness of Bi_2Te_3 in air environment

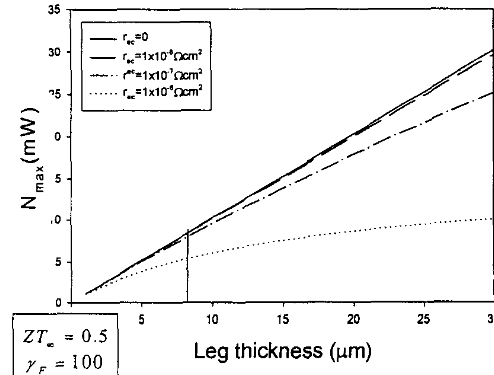

Figure 8: Cooling capacity of the μ-TEC as function of thickness of Bi_2Te_3 in air environment

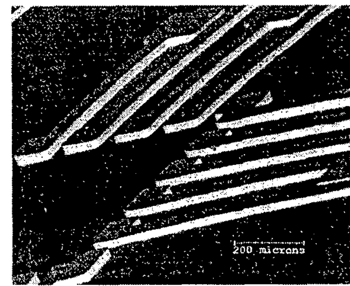

Figure 9: TE (n-Bi_2Te_3) legs grown by electroplating technique

V. μ-TEC fabrication:

As described in the preceding sections, thin and thick TE films are patterned by different techniques. The rest of device fabrication described here applies to both of the TE films and most other TE films of the future as well. Low temperature Au-In eutectic bonding technique is used to connect n- and p-type patterned TE legs. The electric connection layers (Au on

one side and In on the other side) are deposited on both the cold and hot contact regions, but not on the top of TE films, as shown in Fig. 6. As a consequence, the electric contact resistance effect must be considered in the analytic model, shown in Eq. (1). To reduce the heat leakage, the active cooling region is made as a membrane island by removing the silicon substrate under the cooling region by deep reactive ion-etching process.

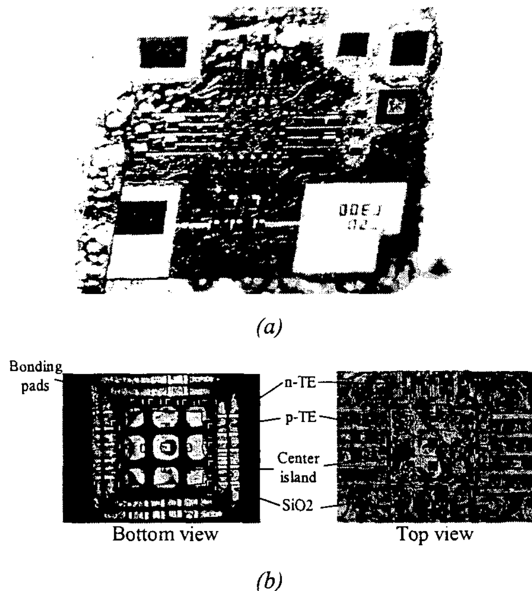

Figure 10: Fabrication of device (a) Si/Ge superlattice μ-TEC, (b) top and bottom view of Si/Ge μ-TEC

A bonded Si/Ge μ-TEC is shown in Fig. 10. From both top and bottom views of Si/GE μ-TEC, it can be seen that the center cooling region is suspended by TE pairs. Alignment needs to be improved to ensure the continuity of TE pairs. The results of temperature measurement, used to make comparison with analytic model, will be reported in the future.

Conclusion

We developed analytical models and used them to predict performance of μ-TEC. The modeling results also led to a clear picture for microdevice configuration and help the development of the fabrication technologies. The MEMS technology is used to develop the fabrication process, which accommodates different TE materials as far as they can be patterned. We are making μ-TEC's with both Si/Ge superlattice and Bi_2Te_3.

Acknowledgments

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